

## **Lead-free Component and Board Identification Standard**

IPC/JEDEC 3<sup>rd</sup> Annual International Conference on Lead-Free Electronics

V. Gupta

Intel Corporation

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## **Acknowledgements**

- ◆ Steve Greathouse Intel
  - ◆ Jack McCullen Intel
  - ◆ Intel Pb-free Team Intel
  - ◆ HDPUG
  - ◆ JEDEC
  - ◆ NEMI
  - ◆ IPC
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## **Agenda**

- ◆ Background
  - ◆ Scope
  - ◆ Timeline
  - ◆ Proposed Marking Scheme
  - ◆ Open Marking Related Issues
  - ◆ Next Steps
  - ◆ Questions
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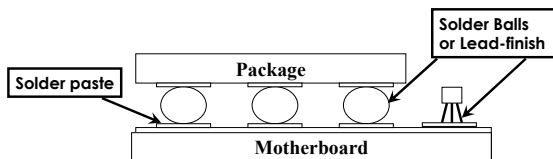
## Background

- ◆ **Conversion to Pb-free electronics has begun**
  - ⇒ Several products are already in the market.
- ◆ **Need to distinguish SnPb and Pb-free components and board products during the transition**
  - ⇒ Prevent product mixing in manufacturing/ inventory
  - ⇒ Different process temperature
  - ⇒ Process compatibility
- ◆ **Marking schemes are inconsistent**
  - ⇒ Some developed for initial products - narrow scope
  - ⇒ Process and real-estate constraints are key influence
- ◆ **There is no proposal for industry standard marking**
  - ⇒ No existing standard/ standard body to cover this scope

## Considerations

- ◆ **An industry standard marking scheme for lead-free component and board products**
  - ⇒ Simple enough to minimize chances for administrative errors
  - ⇒ No major changes to existing marking infrastructure
  - ⇒ Common scheme for both Boards and Components
- ◆ **Focus on 2<sup>nd</sup> level interconnect only**
  - ⇒ Solders that impact board assembly process
  - ⇒ Identify impact on manufacturing
  - ⇒ Keep scope manageable

## Marking Proposal Scope



### WHAT IS INCLUDED:

- ◆ **Component and board lead-free products marking**

## Out of Scope

**WHAT IT NOT INCLUDED:**

- ◆ Is not a "Branding" scheme!
- ◆ Is not a way to identify Pb-free products!
- ◆ 1<sup>st</sup> level interconnect materials are not identified  
*(e.g. flip chip bump, pin attach, multi-chip substrate attach).*
- ◆ Does not include Halogen-free marking  
⇒ Does not impact solder joint performance
- ◆ It is not an endorsement for a particular lead-free option  
⇒ Consideration give to interaction of various solders in board assembly process

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## Marking Standard Development Timeline

- ◆ Agreement with several consortia bodies to develop the proposal  
⇒ NEMI, JEDEC, HDPUG, IPC etc..
- ◆ Proposed timeline
 

⇒ Initial proposal	Feb 2003	
⇒ Obtain industry feedback	March to May 2003	←
⇒ JEDEC Standard draft	April 2003	
⇒ Final Proposal	May 2003	
⇒ Share Proposal with JEITA etc.	Timing TBD	
⇒ JEDEC Ballot	June 2003	
⇒ Standard Release	December 2003	

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## Proposed Marking Scheme

### Solder Material Marking Matrix

#### Identification of Interconnect Material Differences

**2<sup>nd</sup> Level Interconnect Materials – for packages and boards.**

Proposed Mark	Categorization	Material Type <sup>1</sup>
No Mark	Not "ROHS" Compliant	Contains lead
e1	SnAgCu family	e.g.: Sn3-4%Ag0.5-0.9%Cu
e2	Contains Bismuth	e.g.: SnZnBi, SnBi
e3	Other lead free materials	e.g.: SnZn, SnZn-x, Pure-Sn, NiPd, NiPdAu, SnAu, SnSb etc.

**1 Solder balls, lead-finish and solder paste materials only**

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## Next Steps

- ◆ Get industry inputs
  - ◆ Jedec ballot
  - ◆ Standard release
  - ◆ Alignment of international standard bodies
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## Questions??

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